AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method for stabilizing power consumption in a digital logic circuit having the power consumption dependent upon signal transitions, the method comprising:

providing a source signal;

XORing the source signal and a scrambling random signal to generate a scrambled signal;

transmitting the scrambled signal through the digital logic circuit; and

XORing the scrambled signal and a descrambling random signal logically identical to the scrambling random signal.

2. (Original) The method of claim 1, additionally comprising transmitting the scrambling random signal through the digital logic circuit.

3. (Original) The method of claim 0, additionally comprising including the scrambling random signal in the scrambled signal.

4. (Cancelled)

5. (Original) The method of claim 1, additionally comprising storing the scrambling random signal.

6. (Original) The method of claim 1, additionally comprising:

generating the scrambling random signal using a first pseudo-random number generator responsive to a reset signal; and

generating the descrambling random signal using a second pseudo-random number generator responsive to the reset signal.

7. (Original) The method of claim 1, additionally comprising:

generating the scrambling random signal using a self-synchronizing scrambler responsive to the scrambled signal; and

generating the descrambling random signal using a self-synchronizing descrambler responsive to the scrambled signal.

8. (Currently amended) A system for stabilizing power consumption in a digital logic circuit having the power consumption dependent upon signal transitions, the system comprising:

a first exclusive OR (XOR) gate connected to receive a source signal and a scrambling random signal, the first XOR gate generating a scrambled signal; and

a second XOR gate connected to receive the scrambled signal and a descrambling random signal logically identical to the scrambling random signal, the second XOR gate generating a descrambled signal;

wherein the scrambled signal is transmitted through the digital logic circuit.

9. (Original) The system of claim 8, in which the source signal is selected from a data signal and a control signal.

10. (Original) The system of claim 8, in which the scrambling random signal is selected from a true random signal and a pseudo-random signal.

11. (Original) The system of claim 8, additionally comprising a random number generator connected to provide the scrambling random signal and the descrambling random signal.

12. (Original) The system of claim 11, in which the scrambling random signal is transmitted through the digital logic circuit.

13. (Original) The system of claim 11, additionally comprising means for storing the scrambling random signal and means for providing the scrambling random signal to the second XOR gate as the descrambling random signal.

14. (Original) The system of claim 8, additionally comprising:

a first pseudo-random number generator responsive to a reset signal and connected to provide the scrambling random signal; and

a second pseudo-random number generator responsive to the reset signal and connected to provide the descrambling random signal.

15. (Original) The system of claim 8, additionally comprising:

a self-synchronizing scrambler responsive to the scrambled signal and connected to provide the scrambling random signal; and

a self-synchronizing descrambler responsive to the scrambled signal and connected to provide the descrambling random signal.

16. (Currently amended) A system for stabilizing power consumption in a digital logic circuit having the power consumption dependent upon signal transitions, the system comprising:

first gating means for gating a source signal and a scrambling random signal, the first gating means generating a scrambled signal having a first logic state when the logic states of the source signal and the scrambling random signal are equal and having a second logic state when the logic states of the source signal and the scrambling random signal are unequal; and

second gating means for gating the scrambled signal and a descrambling random signal logically identical to the scrambling random signal to generate a descrambled signal having a first logic state when the logic states of the scrambled signal and the descrambling random signal are equal and having a second logic state when the logic states of the scrambled signal and the descrambling random signal are unequal;

wherein the scrambled signal is transmitted through the digital logic circuit.

17. (Original) The system of claim 16, in which the source signal is selected from a data signal and a control signal.

18. (Original) The system of claim 16, additionally comprising means for generating the scrambling random signal and means for generating the descrambling random signal.

19. (Original) The system of claim 16, additionally comprising:

a first pseudo-random number generator responsive to a reset signal and connected to provide the scrambling random signal; and

a second pseudo-random number generator responsive to the reset signal and connected to provide the descrambling random signal.

20. (Original) The system of claim 16, additionally comprising:

a self-synchronizing scrambler responsive to the scrambled signal and connected to provide the scrambling random signal; and

a self-synchronizing descrambler responsive to the scrambled signal and connected to provide the descrambling random signal.

21. (New) A method for stabilizing power consumption in a digital logic circuit, the method comprising:

providing a source signal;

XORing the source signal and a scrambling random signal to generate a scrambled signal;

transmitting the scrambled signal through the digital logic circuit;

passing the scrambling random signal around the digital logic circuit; and

XORing the scrambled signal and a descrambling random signal logically identical to the scrambling random signal.

22. (New) The method of claim 21, additionally comprising storing the scrambling random signal.

23. (New) The method of claim 21, additionally comprising:

generating the scrambling random signal using a first pseudo-random number generator responsive to a reset signal; and

generating the descrambling random signal using a second pseudo-random number generator responsive to the reset signal.

24. (New) The method of claim 21, additionally comprising:

generating the scrambling random signal using a self-synchronizing scrambler responsive to the scrambled signal; and

generating the descrambling random signal using a self-synchronizing descrambler responsive to the scrambled signal.